What is claimed is:

1. A semiconductor memory device comprising:

a word line drive circuit including a drive transistor, which drives a word line;

a circuit for turning said drive transistor OFF after an output of said word line drive circuit reaches a high level; and

a word-line-voltage increasing circuit for increasing a voltage of said word line after said drive transistor turns OFF,

wherein said word-line-voltage increasing circuit includes a coupling capacitor, one end of which is connected to said word line, and a capacitor drive circuit, an output end of which is connected to the other end of said coupling capacitor,

said capacitor drive circuit switches its output from a low level to a high level at a timing when said drive transistor is OFF.

2. The semiconductor memory device according to claim 1 further comprising a memory cell, which is a static memory cell, connected to said word line.

3. The semiconductor memory device according to claim 1, wherein said coupling capacitor includes a line running along said word line.

4. The semiconductor memory device according to claim 3, wherein said line running along the word line has different

length from said word line.

5. The semiconductor memory device according to claim 4 further comprising a predetermined number of memory cell arrangement data arranged in the word-line running direction,

wherein said memory cell arrangement data includes a first memory cell arrangement data which has the word line and the line running along the word line of a memory cell arrangement unit, and a second memory cell arrangement data which has the word line of a memory cell arrangement unit, and does not have the line running along the word line ,

a necessary number of the first memory cell arrangement data to obtain a predetermined value of the coupling capacitor is continuously arranged in the predetermined number of memory cell arrangement data, and the other arranged memory cell arrangement data is the second memory cell arrangement data.

6. The semiconductor memory device according to claim 3, wherein said line running along the word line in said coupling capacitor is formed in the same wiring layer as said word line, and is divided for every one memory cell unit or every two or more memory cell units connected to said word line,

each divided line running along the word line is backed by other wiring line which runs along the word line on an upper layer on or above said word line.

7. The semiconductor memory device according to claim 1, wherein the output of said word line drive circuit is a control

input signal for turning said drive transistor OFF.

8. The semiconductor memory device according to claim 1, wherein the output of said word line drive circuit is an input signal of said capacitor drive circuit.

9. The semiconductor memory device according to claim 1, wherein a writing control signal is provided to said word-line-voltage increasing circuit, said word-line-voltage increasing circuit increases a voltage of said word line only in writing.

10. The semiconductor memory device according to claim 9, wherein a column decoding signal is provided to said word-line-voltage increasing circuit as a control signal,

a signal of a global word line is provided to said word line drive circuit,

a plurality of said word line drive circuits are connected to said global word line,

said column decoding signal selects whether the word-line-voltage increasing circuit is activated or not in wiring.

11. A semiconductor memory device comprising:

a word line drive circuit including a drive transistor, which drives a word line;

a circuit for turning said drive transistor OFF after an output of said word line drive circuit reaches a high level; and

a word-line-voltage increasing circuit for increasing a voltage of said word line after said drive transistor turns OFF,

wherein said word-line-voltage increasing circuit is a switch circuit, which is provided between a voltage supply, which supplies a voltage higher than a power supply voltage supplied to said word line drive circuit, and said word line,

said switch circuit turns ON after said drive transistor turns OFF.

12. The semiconductor memory device according to claim 11, wherein a signal is provided to said switch circuit from the word line drive circuit as an ON/OFF control signal,

said switch circuit includes a level conversion circuit, which changes said signal from the word line drive circuit into the voltage higher than the power supply voltage supplied to said word line drive circuit.

13. The semiconductor memory device according to claim 11, wherein a writing control signal is provided to said switch circuit as an ON/OFF control signal,

said switch circuit responds to the signal from the word line drive circuit only in writing.